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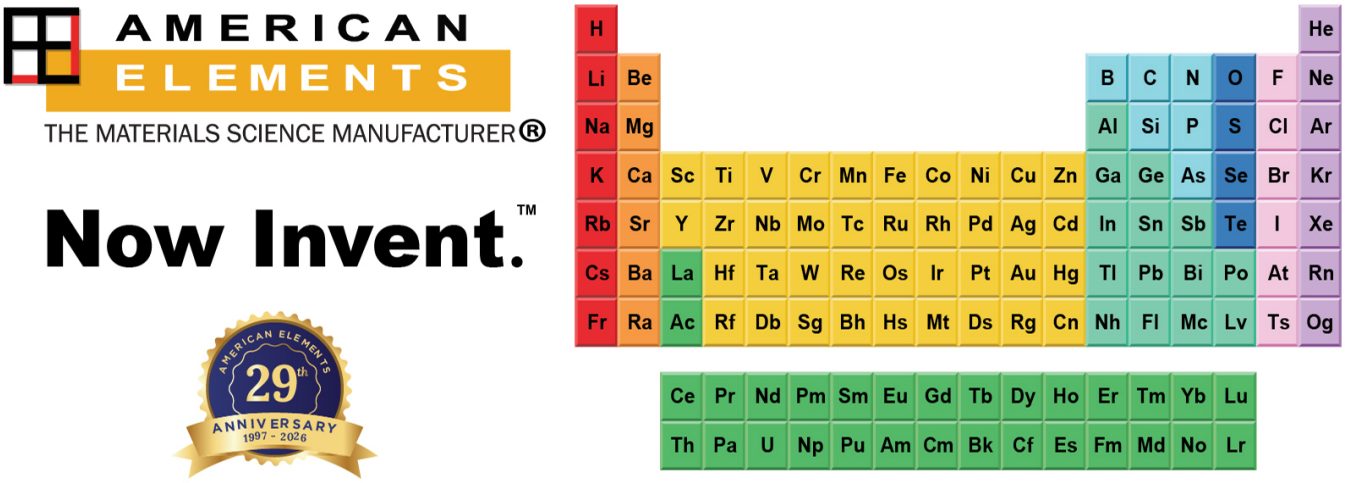
Tuning and experimental assessment of second-order generalized integrator –frequency locked loop grid synchronization for single-phase grid assisted system

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Tuning and experimental assessment of second-order generalized integrator –frequency locked loop grid synchronization for single-phase grid assisted system

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Abstract. The phase-locked loop (PLL) is an essential part of the grid-tied system to synchronize control of converter with grid voltage, particularly affects the converter stability as well as performance under weak grid conditions. During abnormality in a grid, its bandwidth ought to be a11dequately brought down to achieve appropriate disturbance rejection capability with a compromise to slower detection speed. The researchers have done intended work in advanced PLLs to improve phase-angle detection speed by modifying the pre/in-loop filtering stage. A most concerning challenge with the PLLs is the means by which to additionally provide superior dynamic performance and reduced settling time without bargaining stability of system along with the capability of disturbance elimination To overcome this challenge, this paper describes the second-order generalized integrator (SOGI-Frequency Look loop (FLL) which offers filtering capability like band-pass filter, low-pass filter, and notch filter for adaptive frequency tuning as well as an orthogonal signal generation for the grid-tied photovoltaic inverter. The impact of control parameters on their dynamic performance in SOGI-FLL is tabulated from a step response of frequency estimation by taking a frequncy shift. Furthermore, Low-cost DSP based STM32F407VGT the microcontroller is employed to implement a SOGI-FLL to test under adverse grid conditions using Waijung Block-set of SIMULINK/MATLAB. The experimental results of SOGI-FLL have proven superior dynamic performance over type-2 PLLs by choosing the appropriate value of the control parameter of SOGI-FLL.

Keywords: Phase detection, phase-locked loop (PLL), grid synchronization,STM32F407VG microcontroller,WAIJUNGBlock-set

1. Introduction

The phase-lock loop is employed to synchronize its internal voltage controlled oscillator with a grid voltage signal in order to extract phase-angle which, further, utilized by different control system blocks of the photovoltaic converter. The phase-lock loop can estimate angular frequencyω_g, phase angle θ_g,

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and frequency f_g for the control block of grid assisted converter from grid voltage and also ensure the protection of converter against an islanded mode. The zero-crossing detection method was first applied as synchronizing technique for grid assisted photovoltaic system (PV),which uses comparators for finding polarity changes in the grid voltage signal. During abnormalities in grid voltage or the case of weak grids, it had a drawback of multiple zero-crossings detections, further which cause issues for extracting phase-angle ofgrid voltage. Stationary frame PLLs are suitable as well as efficient in single-phase grid assisted PV converter due to the only one voltage signal to synchronize as well as increase in the speed of synchronization in comparison with other methods. Classical PLL systems consist of a multiplier phase detector (PD) that yields an error signal ε_{pd} for the low-pass filter (i.e. loop filter) (LF); which is further created $\omega_e$for the phase-angle extraction. The Phase detector is having an inherent drawback of producing a (2ω) ripple components in ε_{pd} that further proliferates through the Loop Filter [1,2,4].It can be minimized by adding another low-pass filter in a loop that encounters this 2ω term at the cost of reduction in bandwidth and/or phase-margin, slower transient response, and decrease in overall speed of synchronization [1,4-7]. Synchronous frame (DQ) PLLs can be adopted to compute frequency and phase angle as well as transform the grid voltage into DC signals. It can be controlled by a simple PI controller with zero steady-state errors in output while PI regulators cannot be used in the stationary frame. However, DQ PLL requires two signals i.e. a direct signal and an orthogonal signal (quadrature signal) for the computation of frequency and phase angle[10-11]. Therefore, an orthogonal signal is derived from direct signal i.e. sensed grid voltage for the transformation from the stationary to the DQ frame by using different methods such as phase delay filters, differentiation of the input signal, Inverse Park's transform, Hilbert transform, [6-7,14],and the second-order generalized integrator (SOGI)[11-12]. In a phase delays filter, generally two low -pass filters with the 0.707 gain and 45° phase are cascaded and their output further divided with 0.5 to create signal with unity gain and 90° phase[1,4,5].But they can cause inaccuracies to arise as a result of slow varying characteristics of the grid within tolerable range whereas differentiation of the input voltage signal method is having an issue of noise amplification during the generation of the orthogonal signal [19, 20]. This paper describes a second Order Generalized Integrator (SOGI)-Frequency Locked Loop(FLL) method for generating the orthogonal component of a 1Φ and phase-angle exctraction for DQ PLL. By appropriate choice of control parameter values, SOGI-FLL offer band-pass, low pass, band stop filtering along with estimation of phase angle, frequency, amplitude as well as offset parameters. Therefore, it can also eliminate the 2ω ripple without using LPFs; subsequently increase inherent synchronization speed as well as bandwidth as compared with convention PLL. The SOGI-FLL method can be use for a phase-angle detection in the single phase as well as three phase grid tied inverter, active filters in power system. It can also used as stationatary-frame current controller and fundamental component extraction from any voltage or current signal.This paper describes how these additional feedback with appropriate selection of control parameter improve synchronization speeds during grid abnormality, increase robustness against input noise and disturbances, and estimate accurate and non-distorted values phase-angle for the control system.Reference [1-6] implemented SOGI-FLL in single-phase grid assisted PV system, but none of the above have focused the impact analysis of parameter k and γ and their effects in transient and steady-state response SOGI-FLL.In this paper,the Imapct analysis of control parameter is tabulated from step reponse of frequency estimation by taking a frequency shift. paper elaborate an analysis of second order generalized integrator and additional structure extensions that allow estimation of the parameters of a periodic signal.

2. Structure of Second-order generalized integrator (SOGI)

The structure of SOGI, as shown in Figure 1, and their transfer functions in equation (1) & (2) are indicating that two imaginary complex conjugated poles placed at $\pm j\omega_0$ that behaved like resonator oscillating at angular frequency ω_0. This feature offers infinite gain at resonator oscillating at angular frequency, ω_0 as observed from the bode plot of SOGI in figure 2 that can be useful in the implementation of voltage controlled oscillator (VCO) block in PLL.

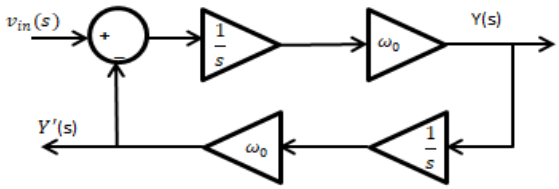


Figure 1. Basic structure of Second-order generalized integrator[11]

$$\frac{\mathrm{Y(s)}}{\mathrm{v_{in}(s)}} = \frac{\omega_0/_s}{1+\frac{\omega_0\omega_0}{s\ s}} = \frac{s\,\omega_0}{s^2+\omega_0{}^2} \tag{1}$$

$$\frac{\mathrm{Y'(s)}}{\mathrm{v_{in}(s)}} = \frac{\mathrm{Y'(s)}}{\mathrm{Y(s)}} * \frac{\mathrm{Y(s)}}{\mathrm{v_{in}(s)}} = \frac{\omega_0}{s} * \frac{s\,\omega_0}{s^2+\omega_0{}^2} = \frac{\omega_0{}^2}{s^2+\omega_0{}^2} \tag{2}$$

$$y(\mathrm{t}) = L^{-1}[Y(s)] = L^{-1}\left[\frac{s\,\omega_0}{s^2+\omega_0{}^2} * \mathrm{v_{in}(s)}\right] = L^{-1}\left[\frac{s\,\omega_0}{s^2+\omega_0{}^2} * \frac{\omega_0}{s^2+\omega_0{}^2}\right] = \frac{1}{2}[t\ \omega_0 \sin\omega_0 t] \tag{3}$$

$$y'(\mathrm{t}) = L^{-1}[Y'(s)] = \frac{1}{2}[\sin\omega_0 t\ \ t\ \omega_0 \cos\omega_0 t] \tag{4}$$

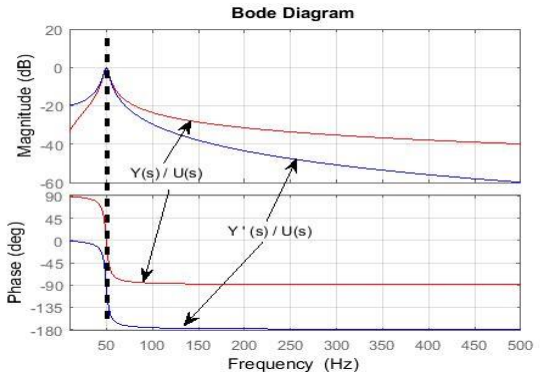


Figure 2. Bode diagram of transfer function (Y(s) / Vin (s))and (Y'(s) / Vin (s))of SOGI

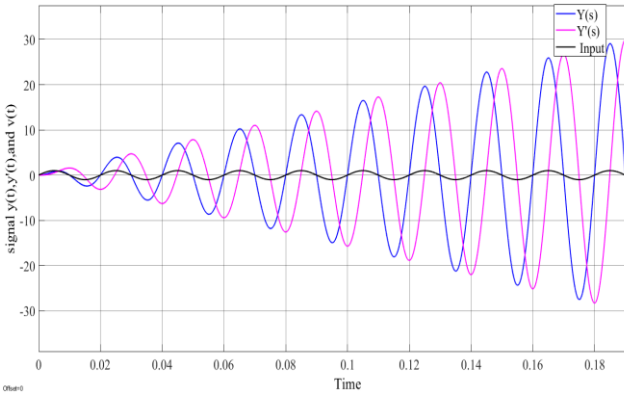


Figure 3. Step response of SOGI

Figure 3 shows the step time response of a SOGI structure as per eq.(3) & eq.(4) with $\omega_0 = 2\pi.50$ rad/s, respectively, that increase the amplitude of output signals which cause unstable system, when a unitary step is applied as input.To prevent the system to be unstable, input to the SOGI structure is modified as weighted k of (where k is the gain parameter of SOGI) the difference of input signal which is nothing but grid voltage$\mathrm{v_{in}(s)}$and unity feedback of output signal Y(s) to the input as shown in Figure 4.

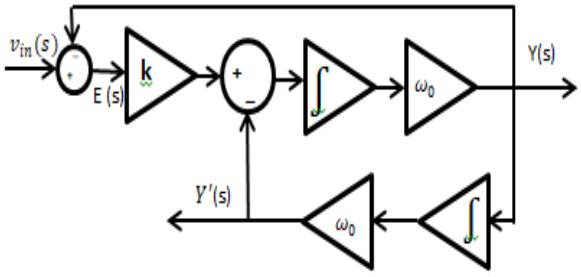


Figure 4. Block diagram of SOGI-OSG

As a result, the transfer functions for $D_v(s)$ and $Q_v(s)$ can be re-written as:

$$D_v(s) = \frac{Y(s)}{\mathrm{v_{in}(s)}} = \frac{k\, s\, \omega_0}{s^2 + k\omega_0 s + \omega_0{}^2} \quad (5)$$

$$Q_v(s) = \frac{Y'(s)}{\mathrm{v_{in}(s)}} = \frac{k\, s\, \omega_0}{s^2 + k\omega_0 s + \omega_0{}^2} \quad (6)$$

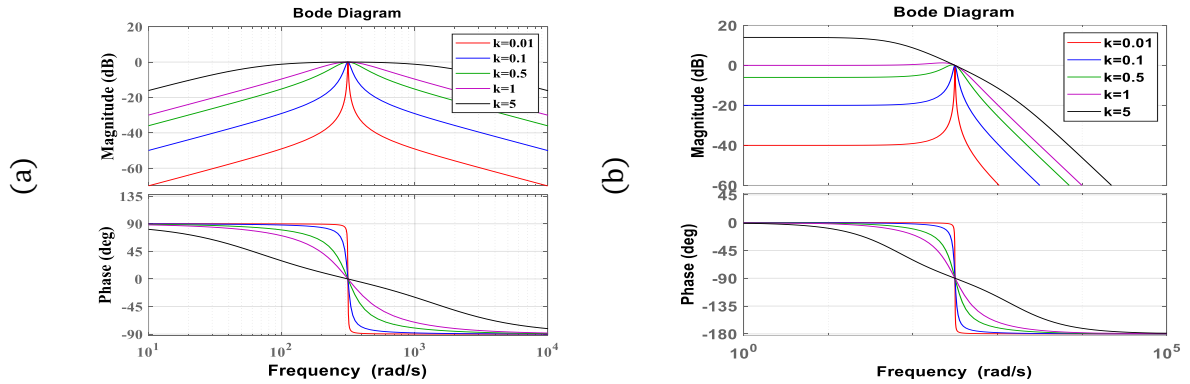


Figure 5 . Bode Diagram of (a) $\boldsymbol{D_v(s)}$, and (b) $\boldsymbol{Q_v(s)}$with different value of k

Bode Diagrams describe band-pass compatible nature of the output *Y*(*s*) (Figure 5) and nature of the output *Y'*(*s*) as low-pass compatible, while phase responses of curves at frequency 50Hz are observed at 0^0 and 90^0respectively which indicates that Y(s) is having90^0 phase lead to *Y'*(*s*) (Figure. 5). Moreover, The magnitude responses of Bode are maintaining 0 dB at the 50Hz fundamental frequency and also attenuating amplitude at 5th and 7th harmonics frequency i.e.250Hz and 350Hz.It is seen from Figure 5 that the transfer function Y(s) and *Y'*(*s*) are able to extract only fundamental components of grid voltage while eliminating harmonics components of grid voltage as second –order band-pass filter.

The SOGI-QSG is employed in SOGI-PLL to generate in-quadrature signal from single phase grid voltage for phase-angle extraction as depicited in Figure 6. The SOGI-PLL locks the phase angle of its internal oscillator to the input grid voltage signal as to when input frequency was detected while detected frequency allowed to remain properly tune SOGI-QSG.

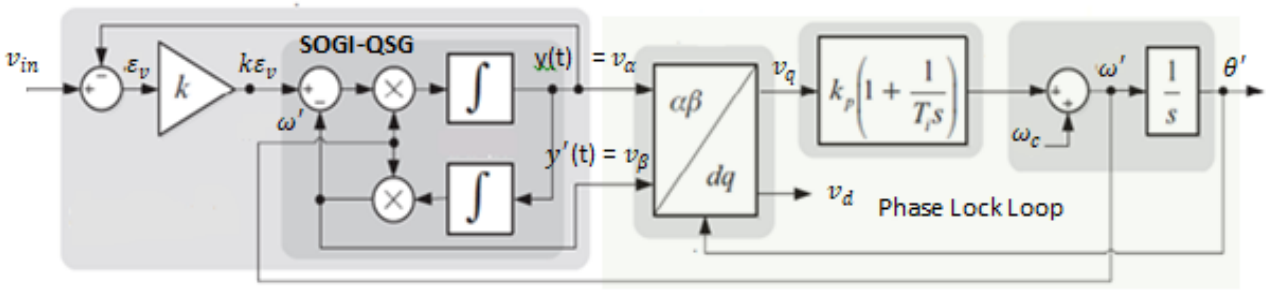


Figure 6.Basic diagram SOGI-PLL[14]

2.1 Frequency locked loop

However, SOGI has an inherent resonate character that can be used as voltage-controlled oscillator which emphasizes to design simple and robust single feedback control loop for an auto-adapting center frequency of SOGI resonator as per the input grid frequency. Frequency Locked Loop, FLL is nothing but the simple and robust extension of SOGI structure as shown in Figure 7. In order to make auto-tunable SOGI-QSG, it should pay attention to the voltage error signal E_v (s), which is nothing but the difference between input v_{in} (s) and output Y(s) and behave as notch filter with zero gain

and180^ophase-angle jump at center frequency as observed from a bode diagram in Figure 8, is described in term of transfer function by

$$E_v(s) = \frac{\varepsilon_{v(s)}}{v_{in(s)}} = \frac{s^2+\omega_0{}^2}{s^2+k\omega_0 s+\omega_0{}^2} \quad (7)$$

The transfer function of $E_v\ (s)$ and $Q_v\ (s)$ gives worthy information for auto-tunable frequency control system by taking common bode diagram of transfer function $E_v\ (s)$ and $Q_v\ (s)$, as depicted in Figure 8.

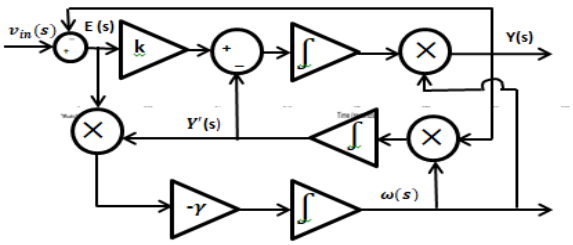


Figure 7.Basic structure of SOGI based Frequency lock loop

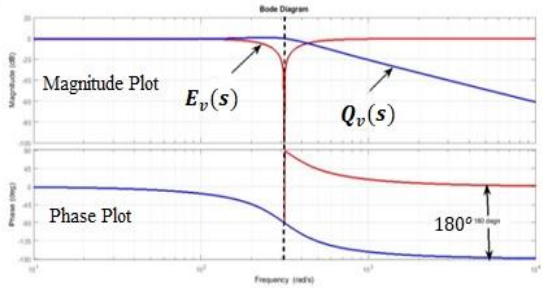


Figure 8. Bode Diagram of the $\boldsymbol{E_v(s)}$ and $\boldsymbol{Q_v(s)}$in an SOGI- QSG

The Bode diagram of transfer function $E_v\ (s)$ and $Q_v\ (s)$reveals that the phase of signals $E_v\ (s)$ and $Q_v\ (s)$ are in a phase when input frequency (ω) lower than SOGI resonance frequency (ω') i.e. $\omega < \omega'$ and out of a phase (180^o phase difference) when $\omega > \omega'$, as indicated in Figure 8. Hence, a frequency error variable ε_f is derived from product of $E_v\ (s)$ and $Q_v\ (s)$, which remain positive when input frequency (ω) is lower than SOGI resonance frequency (ω'), zero when $\omega = \omega'$, and remain negative $\omega > \omega'$ in the SOGI-FLL.Moreover, the frequency locking loop can be designed by using frequency error variable, ε_f and a negative value of frequency loop controller gain,$-\gamma$ as shown in Figure 7. The frequency loop controller gain $(-\gamma)$ is used to achieve DC component of frequency error variable ε_f equal to zero by changing SOGI resonance frequency,ω', until equal to the input frequency, ω.A feed-forward variable, ω_c i.e. nominal value of grid frequency is provided in frequency locking loop to speed up the initial synchronization process. The SOGI-OSG and Frequency locking loop combined a structure diagram known as SOGI-FLL for single-phase grid synchronization system, as shown in Figure 7. The transient and steady-state behavior of the SOGI –FLL mainly depends on a suitable value chosen for control parameters γ and k in order to obtain desired response in the estimation of the frequency and amplitude of input signal.From the Figure 7, the state-space equations are described as:

$$\dot{x} = \begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = Ax+Bu = \begin{bmatrix}-k\omega' & -\omega'^2\\ 1 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}k\omega'\\ 0\end{bmatrix}u \quad (8)$$

$$y = \begin{bmatrix}y\\ y'\end{bmatrix} = Cx = \begin{bmatrix}1 & 0\\ 0 & \omega'\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} \quad (9)$$

$$\dot{\omega}' = -\gamma\ x_2\omega'\ (u - x_1) \quad (10)$$

where $x = [x_1 \quad x_2]^T$ and $y = [y \quad y']^T$ are the state variables and output vectors respectively.
The voltage error signal from state equations in eq.(8) and Figure 7can be written as

$$\tilde{\varepsilon}_v = (u - \tilde{x}_1) = \frac{1}{k\ \omega'}(\dot{\tilde{x}}_1 + \omega'^2\tilde{x}_2) \quad (11)$$

The steady–state frequency error signal$\tilde{\varepsilon}_f$ can be derived as:

$$\tilde{\varepsilon}_f = \omega'\tilde{x}_2\tilde{\varepsilon}_v = \frac{\tilde{x}_2{}^2}{k}(\omega^2 - \omega'^2) \quad (12)$$

The small-signal performance of FLL can be obtained by simplifying $(\omega^2 - \omega'^2) \approx \omega'(\omega' - \omega)$ taken into the consideration of steady –state condition i.e. $\omega = \omega'$

$$\dot{\omega}' = -\gamma\ \tilde{\varepsilon}_f = -\gamma\ \frac{\tilde{x}_2{}^2}{k}(\omega^2 - \omega'^2) \approx -2\gamma\ \frac{\tilde{x}_2{}^2}{k}\omega'(\omega' - \omega) \approx -\frac{\gamma V^2}{k\ \omega'}(\omega' - \omega) \quad (13)$$

A value of γ should be normalized by using feedback and described as:

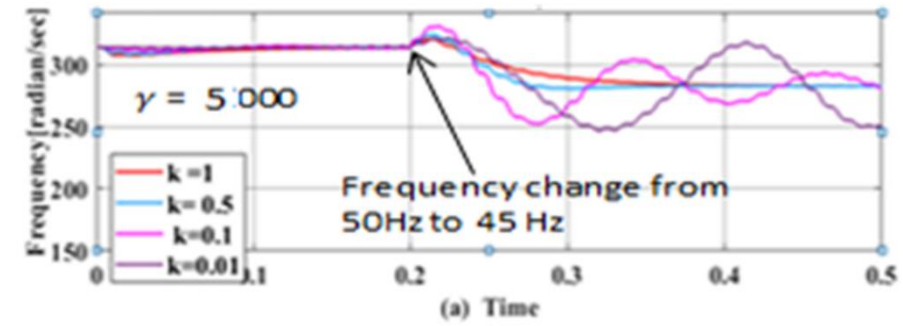
$$\gamma = \frac{k\omega}{V^2}\Gamma \quad (14)$$

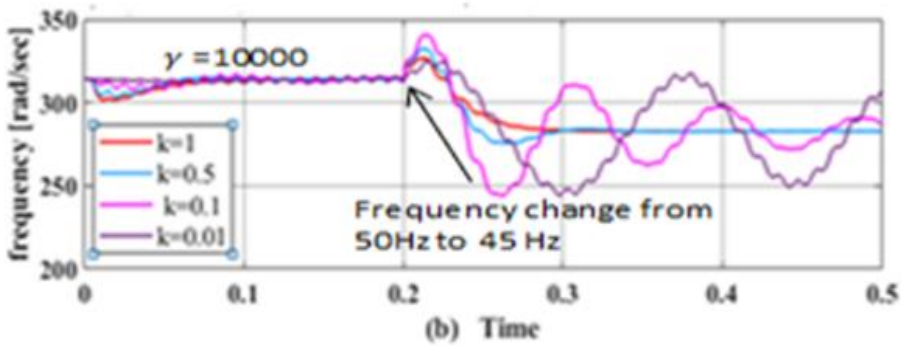
3. Comparative Analysis

Reference [1]-[6] implemented SOGI-FLL in single-phase grid assisted PV system, but none of the above have focused the impact analysis of parameter k and γ and their effects in transient and steady-state response SOGI-FLL. The dynamic performance of frequency estimation in SOGI-FLL is examined by experiencing a -5 Hz frequency step change (i.e. frequency jump (50Hz to 45Hz) and phase angle shift (0^0 to45^0) at 200msec with feed-forward taking initial frequency value i.e. $2\pi * 50$.

Table 1. IMPACT ANALYSIS OF SOGI-FLL

Parameter	Progressive change	Transient response	Steady-state response	Filtering	Settling Time
k	Increasing	Good	Good	Good	Reduce
	Decreasing	Poor	Poor	Poor	Increase
γ	Increasing	Poor	moderate	No effect	Reduce
	Decreasing	Good	Good	No effect	Increase





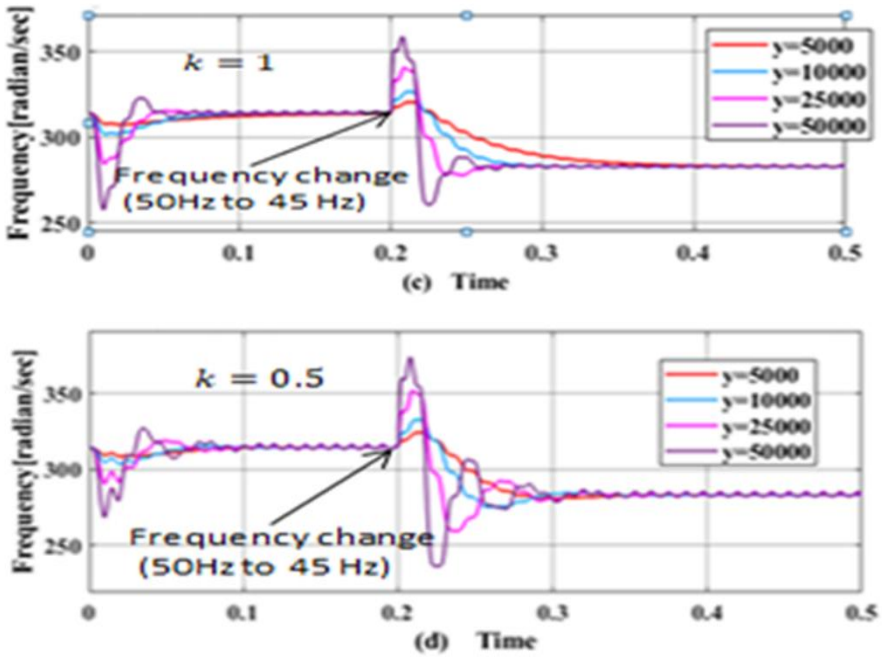


Figure 9.Step response of Frequency Estimation (a) different value of k ,constant value γ=5000, (b) different value of k ,constant value γ=10000, (c) different value of γ ,constant value k=1, and (d) different value of γ ,constant value k=0.5

In Figure 9 (a) & (b), the dynamic response of frequency estimation is observed by taking a progressive value of k and constant value of γ, in the Figure 9 (a) & (b), and progressive value of γ and constant value of k , in Figure 9 (c) & (d). Impact analysis of parameters k and γ in SOGI-FLL have been tabulated from the Figure 9 (a)-(d) in table-1.The para-meter k is used to amplify signal (ε_v) , which affects the transient response and also bandwidth and of SOGI-FLL. The selection of the gain k is compromising between good signal filtering and dynamic response of system (Figure.5 & Figure 9). The selection of γ value is a trade-off between precision of frequency estimation and dynamics of SOGI-FLL. Narrower bandwidth increases the rise time (t_r= 0.35/ BW), further, degrades successive value stabilization of frequency estimation, however, adversely improves the other parameters.

4. Experimental Results

The SOGI-FLL is implemented and tested by using a downscaled STM32F407VGT6 microcontroller and waijung block-set environment in Simulink/Matlab. The discrete- SOGI-FLL model is converted into c code, that further, compiled and dumped into microcontroller by KEIL-IDE (KEIL 4 and above, ST-utility driver) and physical interface USB cable. The STM32F407VGT6 is a low cost, 32-bit microcontroller having 2 Digital analog converters(12bit-DAC) with 168 MHz crystal frequency, and supported by waijung environment (i.e. model-based programming) in the SIMULINK/MATLAB.The experimental results are verified with simulation results to present the effectiveness of SOGI-FLL using model-based programming. The convenient parameter value of SOGI-FLL are chosen as k = 0.5, $\gamma = -5000$,sampling time t_s = 50 usec, and grid voltage frequency f_g = 50 Hz. The DC-offset is generated due to ADC conversion block and other discrete blocks cause uncertainty in phase-detection in SOGI – FLL.However, many researchers presented many improved structures of SOGI-FLL. The SOGI-FLL used along with first-order high-pass filter (i.e known as DC blocker) with cut-off frequency 1-5 Hz to eliminate DC offset without moving toward a complex modification in structure.

For the validation, SOGI-FLL is tested under various cases individually in the experimental set-up as follow:

Test 1: It is conducted on the grid voltage affected by voltage sag of 0.6 p.u,

Test 2: It is conducted on the grid voltage experiences a -5 Hz frequency step change (i.e. frequency jump (50Hz to 45Hz) and phase angle shift (0^0 to 45^0) .

Test 3: It is conducted on the grid voltage affected by harmonics.

In Figure 10, experimental results are obtained to measure settling time of SOGI-FLL on the grid voltage affected by voltage sag of the magnitude 0.6 p.u at t=200 msec .These results are only visible in the Digital oscilloscope have a frequency above 70 MHz and change must be applied after 200msec.

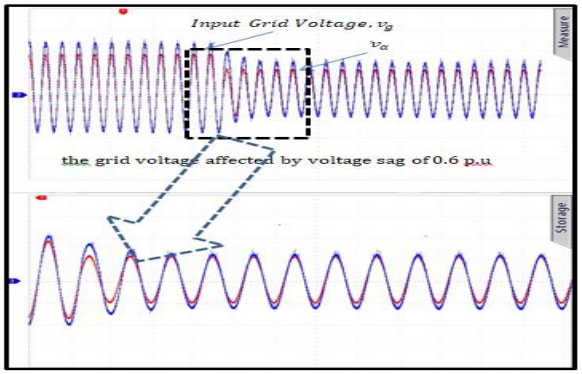


Figure 10. Experimental results: output signal $v_\alpha$of SOGI-FLL with input grid voltage characterized simultaneously dc offset, voltage sag of 0.6 p.u

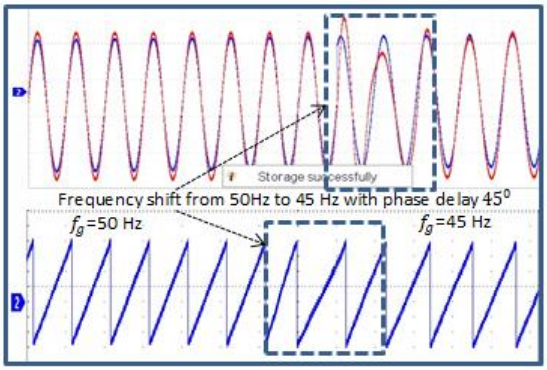


Figure 11. Experimental results: output signal $v_\alpha$of SOGI-FLL with input grid voltage encountered with frequency jump (from 50Hz to 45Hz) and phase angle shift (0^0 to 45^0), and also phase-angle detected by SOGI-FLL

Figure 10 shows that v_α/v' of SOGI-FLL settled down before the third cycle i.e 50 msec when grid voltage affected by sag of 0.6 p.u. As shown in the Figure 11, the dynamic response of SOGI-FLL is evaluated by performing experimental test-2 i.e. grid voltage experiences a -5 Hz frequency step change (frequency jump from 50Hz to 45Hz) and phase angle shift (0^0 to 45^0) at t =500msec. The phase angle shift (from 0^o to 45^o) is intentionally made only to observe frequency change occurs at t =500msec, as shown in figure 18. The frequency and phase- angle detected by SOGI-FLL are settled down before the third cycle observe from the time instant at which the frequency shift made in grid voltage.

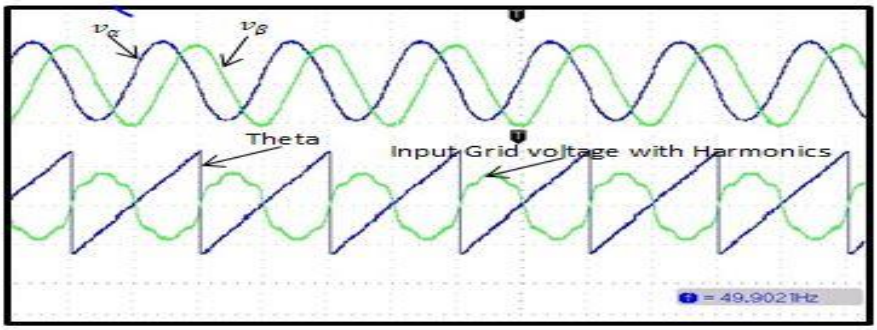


Figure 12. Experimental results: output signal v_α&$v_\beta$of SOGI-FLL with input grid voltage effected by harmonics component, and phase angle shift (0^0 to45^0), and also phase-angle detected by SOGI-FLL

Due to the unavailability of AC grid simulator, this test is conducted by generating sin wave inside SIMULINK/MATLAB and frequency controlled by externally through the ADC pin of a microcontroller. As shown in Figure 12, the dynamic response of SOGI-FLL is evaluated by performing experimental test-3 i.e. grid voltage affected by 3rd, 5th and 7th order harmonics with proportional amplitudes of 35%, 15%, and 8%, respectively, with respect to fundamental grid voltage.The SOGI-FLL is confirmed as immunity to distorted grid voltage as presented in Figure 12. Figure 12 shows that the detected phase-angle free from the harmonics distortion present in the supply voltage as well as the 100Hz frequency component in phase-angle.Besides, SOGI-QSG is experimentally proven as band-pass filter through output signal of SOGI-FLL i.e. v_α/v' and v_β/qv'also free from the effect of harmonics distortion as shown in figure 19. The SOGI-FLL works in the same fashion even in the situation when the grid voltage is affected by multiple abnormalities.

5. Conclusions

In this paper, attention was paid to estimate the frequency and further phase angle detection by tan-arc method for changing frequency and voltage of single-phase utility. The additional structure in a second-order generalized integrator (SOGI) provides a disturbance rejection capability along with selective harmonics filtering ability, informal to design and implement on wijung-block set of SIMULINK/MATLAB environment to perform at desired bandwidth.The main challenging in a design point view is to identify the operative conditions, and further estimate suitable control parameters for SOGI-FLL. The selection of appropriate control parameters is a trade-off between the dynamic response, filtering capability and the desired accuracy in detection of frequency and phase angle especially during a non-ideal grid conditions for single-phase grid-tied inverter. The second challenging part is to create the synchronization process adaptive as well as a fast dynamic response to frequency changes that may happen during the power balancing in the grid system. The practical design constrains of a non-linear system FLL was discussed in this paper. Experimental results have justified that rejection of dc offset achieve through a high-pass filter with cut-off frequency1-5Hz in place of complex DC offset rejection PLL method. It is also proven that appropriate selection of control parameters provides a desire settling time, improves bandwidth, good filtering capability for the lower order harmonics, accurately estimate frequency and a superior response during grid abnormality.

6. References

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